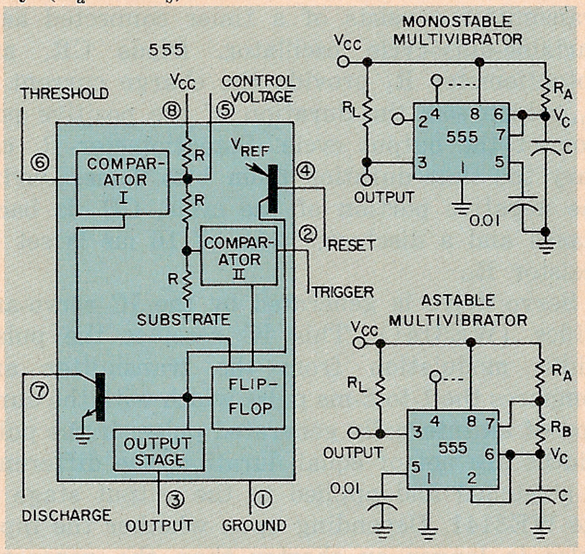
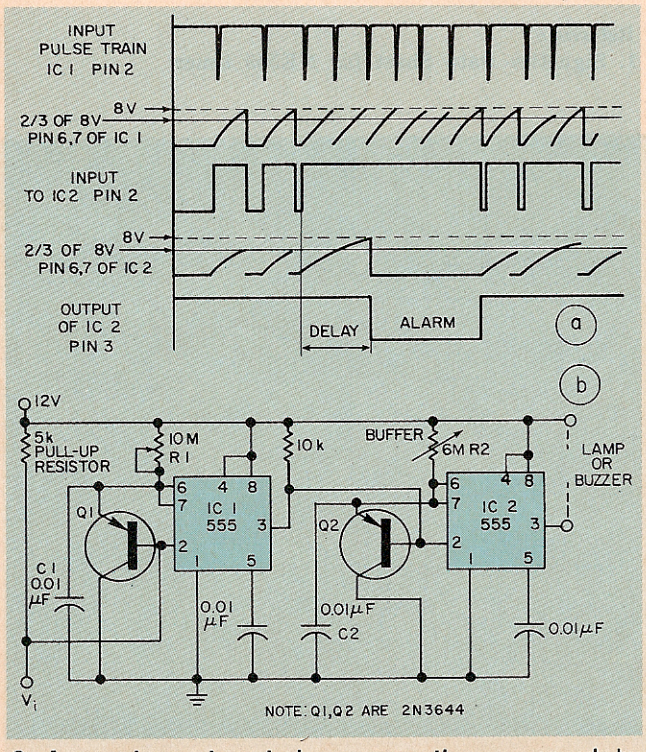
The 555: How it works

The 555 monolithic IC contains two comparators, a flip-flop, a high-current output stage, a voltage reference and a resistive divider. The flip-flop is controlled by the comparators, and the comparators are referenced to V_{cc}. Comparator II sets the initial state of the flip-flop. It is controlled by an external threshold signal (referenced to one-third of V_{cc}) that is applied to pin 2. The flip-flop, in turn, controls the state of the output. A negative-going pulse (of magnitude less than one-third V_{cc}), applied to the trigger input, sets comparator II and the flip-flop.

Two of the fundamental modes of operation are as a monostable one-shot and as a free-running multivibrator (astable). For the monostable mode, a negative going pulse from V_{cc} to less than one-third of V_{cc} at pin 2 changes the flip-flop state. This sends the output high and removes a short-circuit from capacitor C. The voltage across C (V_c) then rises exponentially until it reaches two-thirds of V_{cc}. The time-constant (τ) is determined by R_a multiplied by C. Therefore the charge time is $1.1(R_aC)$. When V_c reaches two-thirds of V_{cc}, comparator I resets the flip-flop and the output again goes low.

The astable circuit is a bit more complex. Resistors R_a, R_b and capacitor C determine the various time constants. When power is turned on, pin 2 sees a low signal and thus removes the short from C. The capacitor then starts charging—the time, t_1, required for C to charge equals $0.685(R_a + R_b)C$. When V_c reaches two-thirds of V_{cc}, the output goes low, and C discharges through R_b and pin 7 until it reaches one-third of V_{cc}. The discharge time, t_2, equals $0.685(R_bC)$. Thus the total period, T, equals $t_1 + t_2$ or 0.685 times $(R_a + 2R_b)C$, and the frequency of oscillation is given by the inverse of T. The pulse duty cycle, D, equals R_b divided by $(R_a + 2R_b)$.[1]





2. **A speed warning device senses the car speed** by comparing the frequency of pulses generated by the rotating wheel. The generated pulse train (a) is processed by the two timer circuit (b) and activates an alarm signal if the speed is too high.

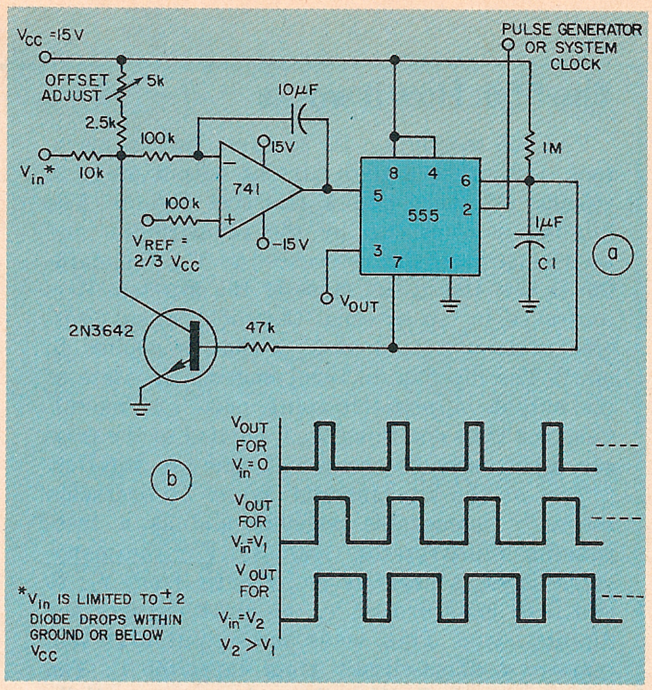
of the tachometer circuit, Fig. 1, and are shaped and clamped by R_1 and CR_1. They are then passed on to the trigger terminal of the timer by C_i. Triggering of pin 2 causes the output of the timer to go high for a period determined by

$$T = 1.1\ (R_4C_2).$$

During this time diode CR_2 is back-biased and resistors R_5 and R_6 provide a calibrated current to the meter. After the time duration elapses, pin 3 goes low, shunting all current around the meter. The ratio of the time for which current flows through the meter to the time for which it is shunted to ground provides an accurate meter reading of engine rev/min. For a V-8 engine, the frequency of pulses at the ignition points is four times the engine rev/min—since the points close eight times per revolution of the camshaft and the engine runs at twice the speed of the distributor shaft. A constant current must be applied to the meter during the one-shot period. This is supplied by the vehicle's electrical system via R_7, C_3 and a 9-V zener, CR_3.

Voltage-to-pulse-duration converter

The circuit in Fig. 3a can convert a voltage level to a pulse duration by integrating the input voltage and comparing its value with the charge on C_1. The timer is set up so that it operates in a monostable mode when no voltage is present at the input. When the input voltage increases, the width of the output pulses increases, but the frequency of the pulse train input to pin 2 remains the same (Fig. 3b). Basically this circuit is a dual-slope integrator and has an accuracy of better than 1%. Possible uses occur in data-acquisition and telemetry.



3. **Voltage levels can be converted** to pulse durations by combining an op amp and a timer IC. Accuracies to better than 1% can be obtained with this circuit (a) and the output signals (b) still retain the original frequency—independent of input voltage.

Servo system controller

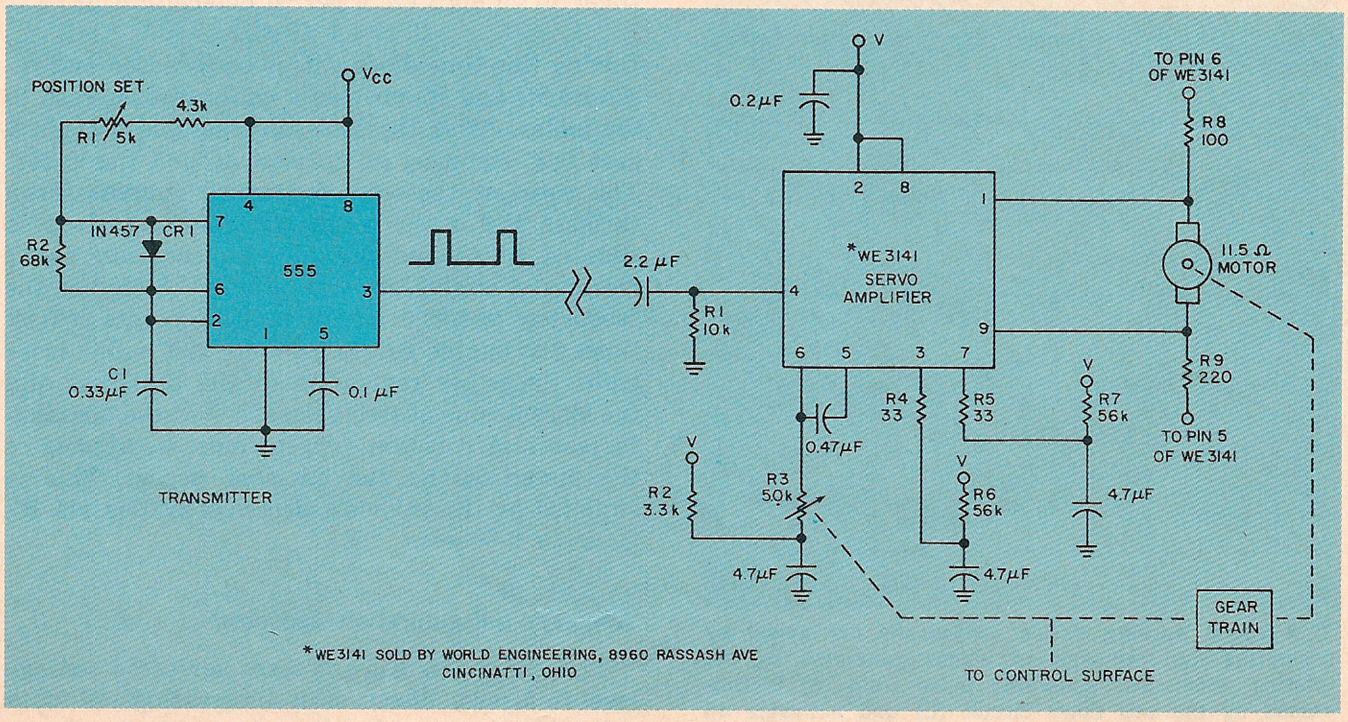
In the motor controller shown in Fig. 4, the transmitter consists of a timer connected as a variable-duty-cycle oscillator. Diode CR_1 and potentiometer R_1 provide the charge current to C_1, which sets the duration of the positive portion of the output cycle. Potentiometer R_1 can vary the time duration from 1 to 2 ms. During the negative portion of the cycle, CR_1 is back-biased and a discharge time of 16 ms is set by resistor R_2.

Servo drive is generated by the IC servo-amplifier (WE3141). This IC receives the pulse-width modulation from the transmitter and compares the 1-to-2-ms pulse width with the duration of an internally generated pulse. If the pulse widths are not of equal duration, the difference is stretched and applied to the output stage of the WE3141. Depending upon whether the input pulse is longer or shorter than the generated pulse, the motor will be driven either clockwise or counterclockwise, to adjust the internal pulse width to match that of the transmitter.

Resistors R_4 and R_5 set the null point of the amplifier. The 33-Ω values allow a null period of about 4 to 5 µs. This hysteresis is necessary to prevent the system from hunting. This type of circuit is useful in a wide range of remote-control systems. ■■

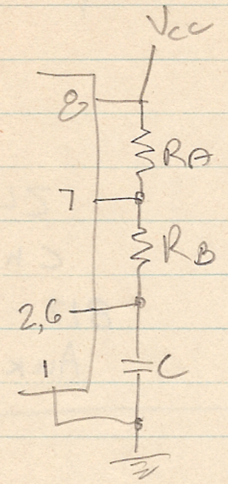
Reference

1. Signetics Data Sheet for NE555 timer.



4. **To remotely control a servo-motor,** the 555 needs only six extra components.

R 555 Calculation for Astablish
(free running)



output Hi

$T_H = .7(R_A + R_B)C$

output Lo

$T_L = .7(R_B)C$

$f = \frac{1}{T} = \frac{1.44}{(R_A + 2B_B)C}$

---

for: f = 10 hz   and T_H = 30 ms

$C = .2 \times 10^{-6}$ fd

$10 = \frac{1.44}{(R_A + 2R_B) \times .2 \times 10^{-6}} = \frac{1.44 \times 10^6}{.2(R_A + 2R_B)}$

$(R_A + 2R_B) = \frac{1.44 \times 10^6}{.2 \times 10} = 7.2 \times 10^5$

$= 720,000\ \Omega$

$T_H = .03 = .7(R_A + R_B) \times .2 \times 10^{-6}$

$T_L = .10 = .7(R_B) \times .2 \times 10^{-6}$

$R_B = \frac{.10}{.14} \times 10^6 = .7 \times 10^6$ or 700K Ω

or

$T_L = .02 = .7(R_B) \times .2 \times 10^{-6}$

$R_B = \frac{.02}{.14} \times 10^6 = .14 \times 10^6 = 140K\ \Omega$

Circuit provides slow auto-wiper cycling, with one to 20 seconds between sweeps

An all-solid-state automobile wiper-control circuit allows the windshield wiper to sweep at selected frequencies from once a second to once every 20 seconds. The circuit uses one IC, two silicon transistors and seven discrete components.

Circuit timing is determined by a 555-timer IC and its external parts, R_A, R_B and C. Transistor Q_1 is switched on when V_1 goes LOW, and npn transistor Q_2 also turns on. The mechanical park switch takes over and conducts the motor current until one cycle of wiper motion is complete. At wiper park, the park switch opens and stops the wiper.

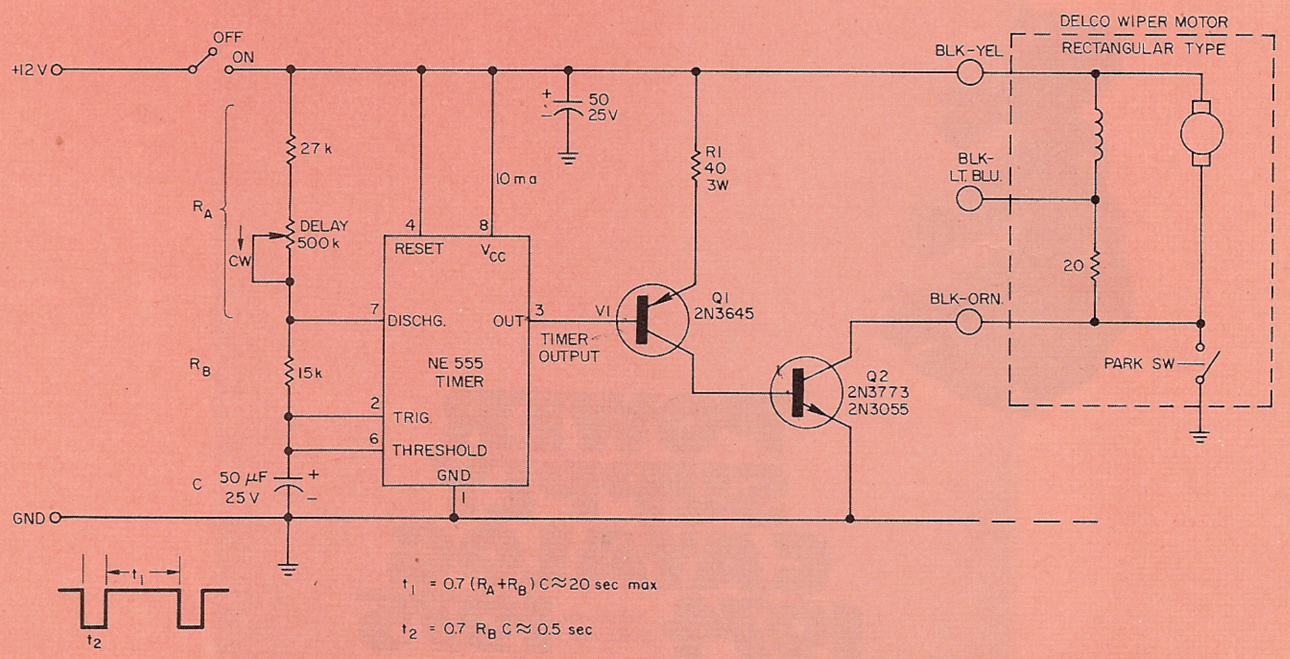
Transistors Q_1 and Q_2 conduct for only about 0.5 s. They do not conduct again until the next timer pulse. The delay between pulses is adjusted with the 500-kΩ delay resistor.

Resistor R_1 limits the current into Q_1 and the base of Q_2. The peak collector current into Q_2 is about 3 A. Since the duty cycle is normally very low, little heating occurs.

This circuit is in use on a GM-Delco rectangular-motor wiper system.

Paul Galluzzi, Electrical Engineer, P.O. Box 352, Beverly, MA 01915.

CIRCLE NO. 313



In this windshield wiper system, voltage V_1 is a 0.5-s pulse—just long enough to move the wiper off the park switch. The wiper then executes one sweep and reparks until the next pulse occurs.

IFD Winner of August 16, 1974

Donn Soderquist, Application Engineer, and Jerry Zis, Mktg. Mgr., Precision Monolithics, 1500 Space Park Dr., Santa Clara, CA 95050. His idea "Successive Approximation A/D Converter Uses Three ICs and Costs Under $25" has been voted the Most Valuable of Issue Award.

Vote for the Best Idea in this issue by circling the number for your selection on the Information Retrieval Card at the back of this issue.

SEND US YOUR IDEAS FOR DESIGN. You may win a grand total of $1050 (cash)! Here's how. Submit your IFD describing a new or important circuit or design technique, the clever use of a new component or test equipment, packaging tips, cost-saving ideas to our Ideas for Design editor. Ideas can only be considered for publication if they are submitted exclusively to ELECTRONIC DESIGN. You will receive $20 for each published idea, $30 more if it is voted best of issue by our readers. The best-of-issue winners become eligible for the Idea of the Year award of $1000.

Single part minimizes differences in monostable and astable periods of 555

A single inexpensive component—a diode or a resistor—can minimize the difference between monostable (one-shot) and astable (free-running oscillator) periods of a 555 timer. When the 555 timer is used as an oscillator, the timing capacitor normally charges from 1/3 V_{cc} to 2/3 V_{cc} to provide an output period of 0.69 RC. However, when used as a one-shot, or when strobed via the reset input, the capacitor must normally charge from zero volts to 2/3 V_{cc}, and a longer period of 1.1 RC is produced.

In the figure, the solid lines show the conventional circuit arrangement for the timer. The switch S selects either the astable or the monostable configuration. Either a resistor R_3 or diode CR, shown dotted, may be added to equalize the timing periods.

A 1N662 diode, placed between pins 3 and 5, pulls down the pin-5 reference voltage to about 0.9 V each time the output goes LOW. Thus the timing capacitor C must now drop to approximately 0.45 V before the level at pin 2 can trigger another output pulse. The capacitor therefore starts to charge from near ground level in both the astable and monostable modes, and the periods agree within 5%.

The advantage of the diode method is that no computations or high-accuracy components are required to provide close matching of pulse widths. Also single potentiometer control of pulse widths is still possible. However, the lower threshold, and therefore the pulse width, depends on the diode's offset and drift characteristics.

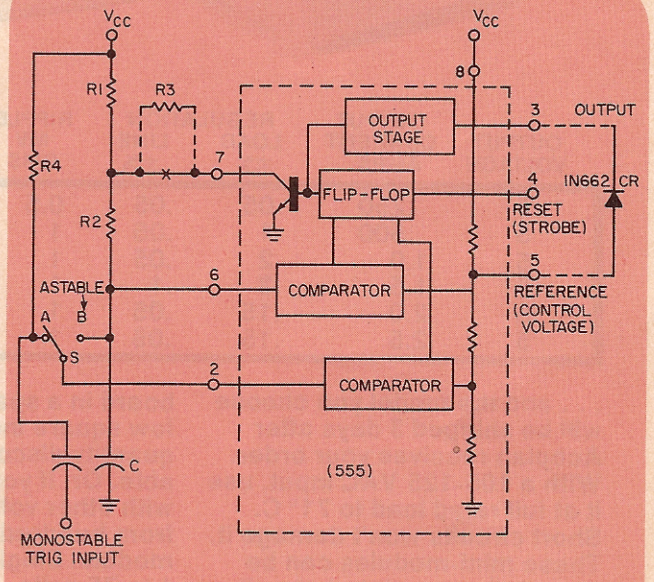
In a second method, resistor R_3 forces the monostable period to approach that of the astable when it prevents the timing capacitor from discharging completely. Careful adjustment of the voltage divider formed by R_1 and R_3 permits the timing-capacitor voltage to drop only far enough to trigger a new pulse. The timing capacitor starts to charge from about 2/3 of the supply voltage in both the monostable and astable modes.

The advantage of the resistor method is that the periods of the two modes are governed by the adjustment of R_1 and R_3. Thus the periods can set very close to each other, and a bypass capacitor to ground can be placed on pin 5—as is done normally. Also the resistor method does not introduce the temperature drift of a diode, and the match of pulse widths tends to remain constant with supply-voltage variations.

One disadvantage is that the value of R_1 cannot be varied to control pulse period without adjustments to R_3 also. In addition, careful consideration of the tolerances of both internal and external voltage-divider resistances is required to attain close pulse-period matching. A cursory analysis shows that 5% resistors of 4.7-kΩ and 1.5-kΩ for R_1 and R_3 yield pulse periods matched to about 20%.

One-percent resistors would allow considerably closer matching. The resistor method is best when high stability is required, or when it is desirable to bypass or to modulate pin 5, and when it is not necessary to have a continuously adjustable pulse width.

Arthur R. Klinger, 3245 Stuff Dr., Orlando, Fla. 32809. CIRCLE NO. 318



The addition of a single component—R_3 or CR— makes the 555 timer's monostable and astable periods almost equal.

powering the 555 from a 5 v supply and using it to drive TTL logic. Occasionally, a step in the output waveform that occurs at the TTL threshold band causes false triggering of the driven circuit. The difficulty can be avoided by adding a 1000 pf capacitor from the output to ground. This lowers the level at which the step appears and removes it from the TTL threshold zone.

In some applications, the 555 can be used as a relay driver. This could be dangerous if the circuit is not connected properly. Driving the load isn't the problem. The difficulty occurs when the relay is deactivated. The collapsing magnetic field of the coil produces a back emf that can cause the tuner to latch up. The solution is to add protection diodes (Fig. 5). Diode D_1 shorts out the reverse emf generated by the collapsing magnetic field. However, a negative voltage equivalent to one diode drop can appear between the timer output and ground. Diode D_2 prevents this. Diode D_2 isn't needed if the relay is connected to V_{CC} rather than ground.

Conversion to an oscillator

The timer can readily be converted into an oscillator (Fig. 6). To convert the monostable circuit into an astable one, a resistor RB is added between the discharge and threshold terminals. Retriggering is accomplished by connecting the trigger input to the threshold terminal. With this circuit, the capacitor charges with time constant $T = 0.693\ (R_A + B_B)C$ until the voltage reaches two-thirds V_{CC}. Then the capacitor discharges with time constant $T = 0.693\ R_BC$ until the capacitor reaches one-third V_{CC} and the cycle repeats.

For this oscillator, the duty cycle (ratio of ON time to total time) is:

$$\text{Duty Cycle} = \frac{R_A + R_B}{R_A + 2R_B}.$$

With this circuit, the duty cycles range from about 50% to 100%. By adding a diode D_1 (Fig. 6), the duty cycle can be modified to give a wider range:

$$\text{Duty Cycle} = \frac{R_A}{R_A + R_B}.$$

When using these configurations, the total resistance $R_A + R_B$ should not exceed 20 megohms. This insures that the comparator input current that must be supplied through $R_A + R_B$ will not effect the timing.

The 555 timer includes a direct lead into the two-third V_{CC} point of the internal divider. This "control" terminal can be modulated with an ac signal to provide an output that is pulse position modulated (oscillator mode), or pulse width modulated (one-shot mode). When this connection isn't used, the IC lead can act as an antenna, picking up signals and changing the time interval. It should be bypassed to ground with a 0.01 μf capacitor.

A reset connection is also provided. When this isn't used, it should be tied to V_{CC}. When used, the voltage should first be dropped to below 0.4 v to reset the timer, then raised to greater than 1 v. Between 0.4 v and 1 v, the device is in an indeterminate state.

Operating a 555 timer at elevated temperatures can be a tricky problem, particularly if appreciable current output is required. For example, will the 555 operate at 125°C when powered from a 12 v supply driving a 60 ma load? To answer this, it is necessary to know, not only the maximum operating die temperature (150°C), but also the thermal resistance θja of the 8 lead TO-5 metal can (0.15°C/mw).

Total dissipation of the device must first be calculated. For 12 v operation, the typical quiescent current is 10 ma, causing 120 mw dissipation. For this application, dissipation of the output structure is approximately 1.7 v times the 60 ma load current, or 102 mw. So the total dissipation is (120 + 102) or 222 mw.

To convert this to a temperature derating, multiply the power dissipation times θja.

$$(222\text{ mw})\ (0.150°\text{C/mw}) = 33.3°\text{C}.$$

The maximum temperature is:

$$(150°\text{C}) - (33.3°\text{C}) = 116.7°\text{C}.$$

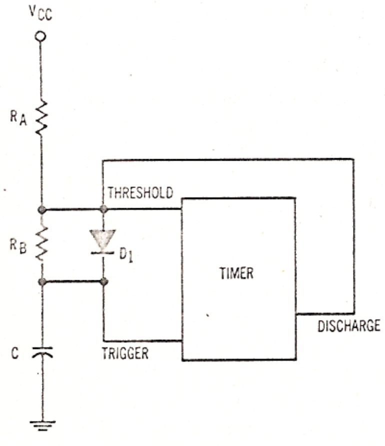


Fig. 6. A timer can be connected as an oscillator by simply adding a resistor R_B and connecting the trigger and threshold inputs together. Adding diode D_1 extends the duty cycle range.

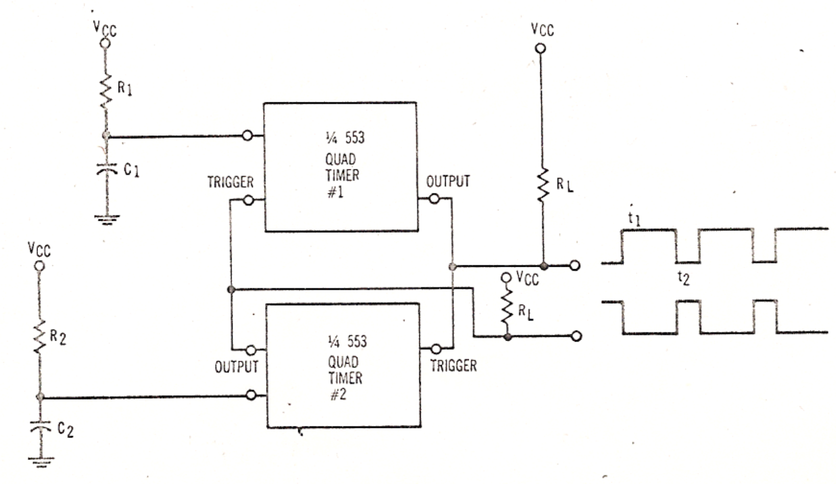


Fig. 7. Two sections of a quad timer can be connected together to form an oscillator. The time constants of each section are adjusted to set the frequency and duty cycle.

applications information

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot (*Figure 1*). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

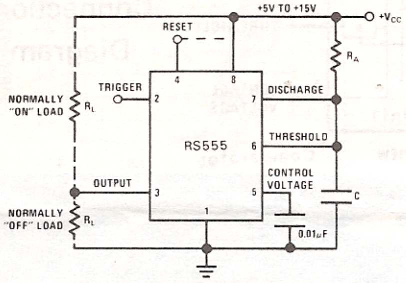


FIGURE 1. Monostable

The voltage across the capacitor then increases exponentially for a period of $t = 1.1\ R_A C$, at the end of which time the voltage equals 2/3 V_{CC}. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. *Figure 2* shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing internal is independent of supply.

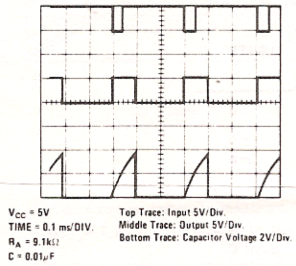


FIGURE 2. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

Figure 3 is a nomograph for easy determination of R, C values for various time delays.

ASTABLE OPERATION

If the circuit is connected as shown in *Figure 4* (pins 2 and 6 connected) it will trigger itself and free run as a

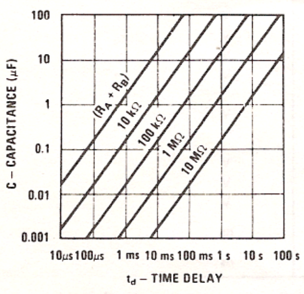


FIGURE 3. Time Delay

multivibrator. The external capacitor charges through $R_A + R_B$ and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.

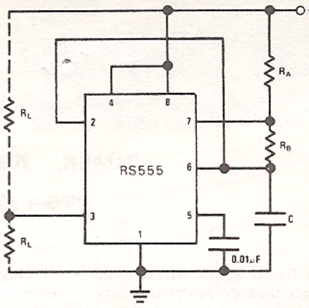


FIGURE 4. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Figure 5 shows the waveforms generated in this mode of operation.

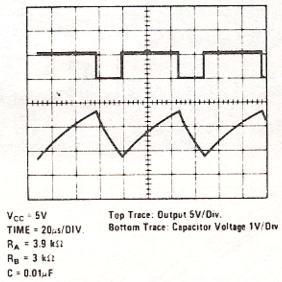


FIGURE 5. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693\ (R_A + R_B)\ C$$

And the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)\ C$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)\ C$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2\ R_B)\ C}$$

Figure 6 may be used for quick determination of these RC values.

The duty cycle is:

$$D = \frac{R_B}{R_A + 2R_B}$$

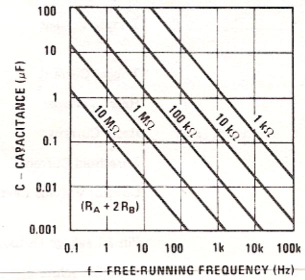


FIGURE 6. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of *Figure 1* can be used as a frequency divider by adjusting the length of the timing cycle. *Figure 7* shows the waveforms generated in a divide by three circuit.

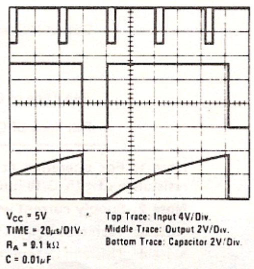
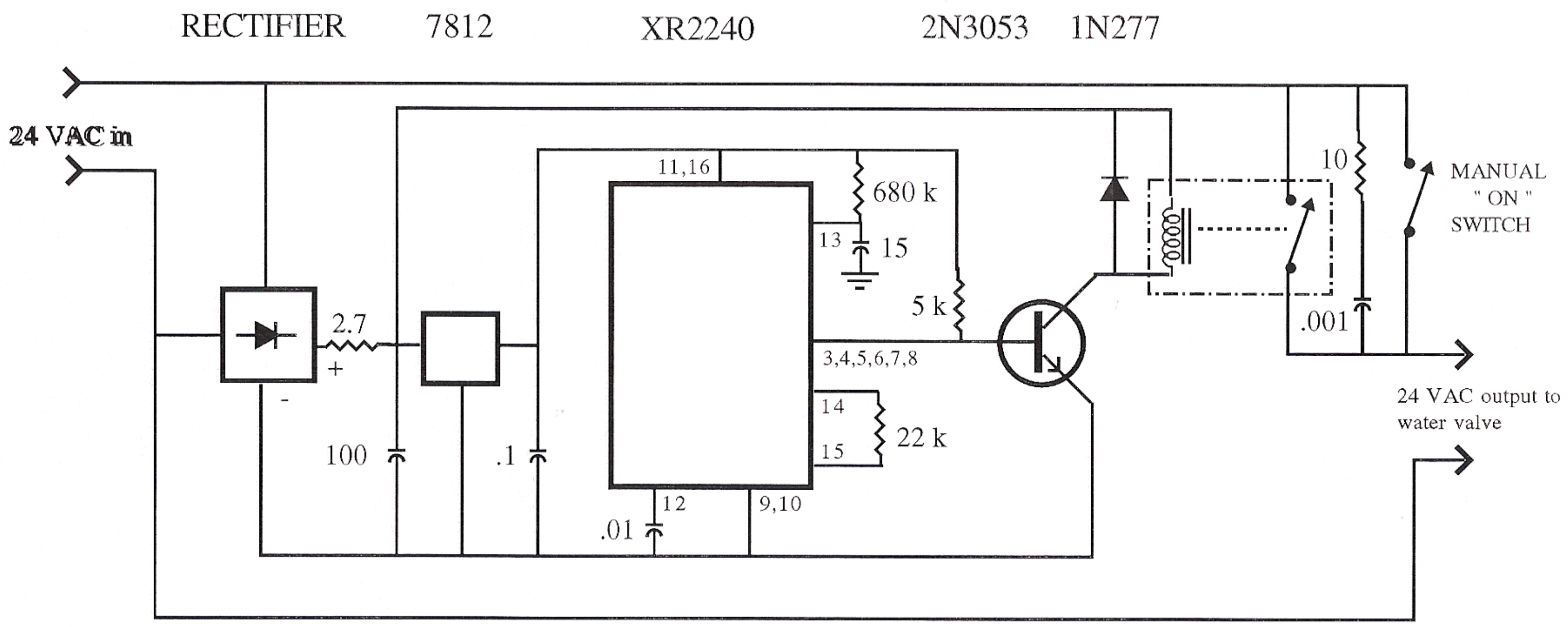


FIGURE 7. Frequency Divider



note: all capacitor values are given in uf.

Cycle Timer shown set up for approximately one minute "ON" each hour

E-C-TEK 107 Gibbon Drive Harvest, AL 35749
WATERING TIMER

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